

Fig. 1
(Prior Art)

Fig. 2

FIG. 2 is a block diagram of a system for processing video data. The system includes a Graphics Controller (208) and an HDTV Encoder (224). The Graphics Controller (208) outputs a Clock signal (212), Input Data (210), a second Clock signal (216), a VSYNC Signal (264), an HSYNC Signal (262), and a Blanking Signal (266) to the HDTV Encoder (224). The HDTV Encoder (224) contains four DACs (246, 248, 250, 252). The DACs 246, 248, and 250 output signals 254, 256, and 258 respectively to an HDTV Monitor (298). The DAC 252 outputs a signal 260 to the HDTV Monitor (298).

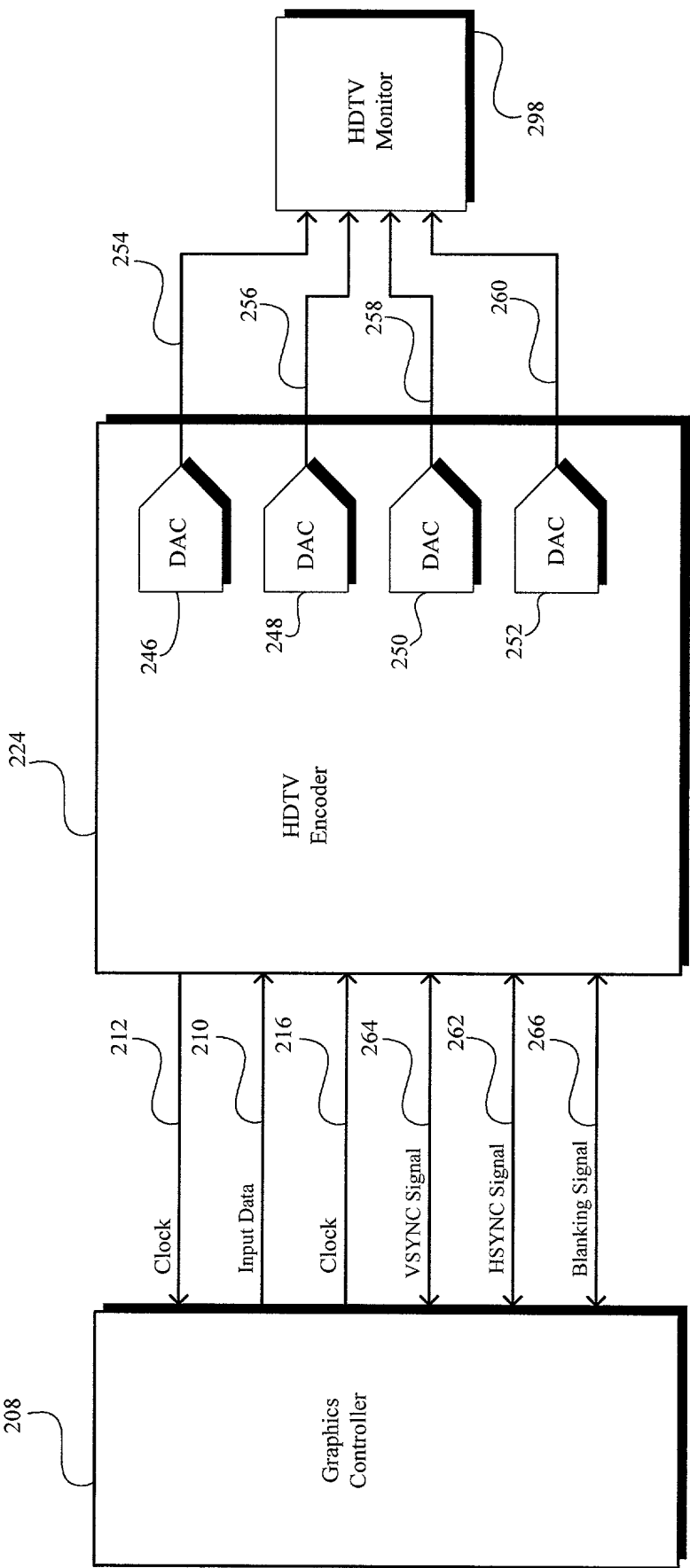
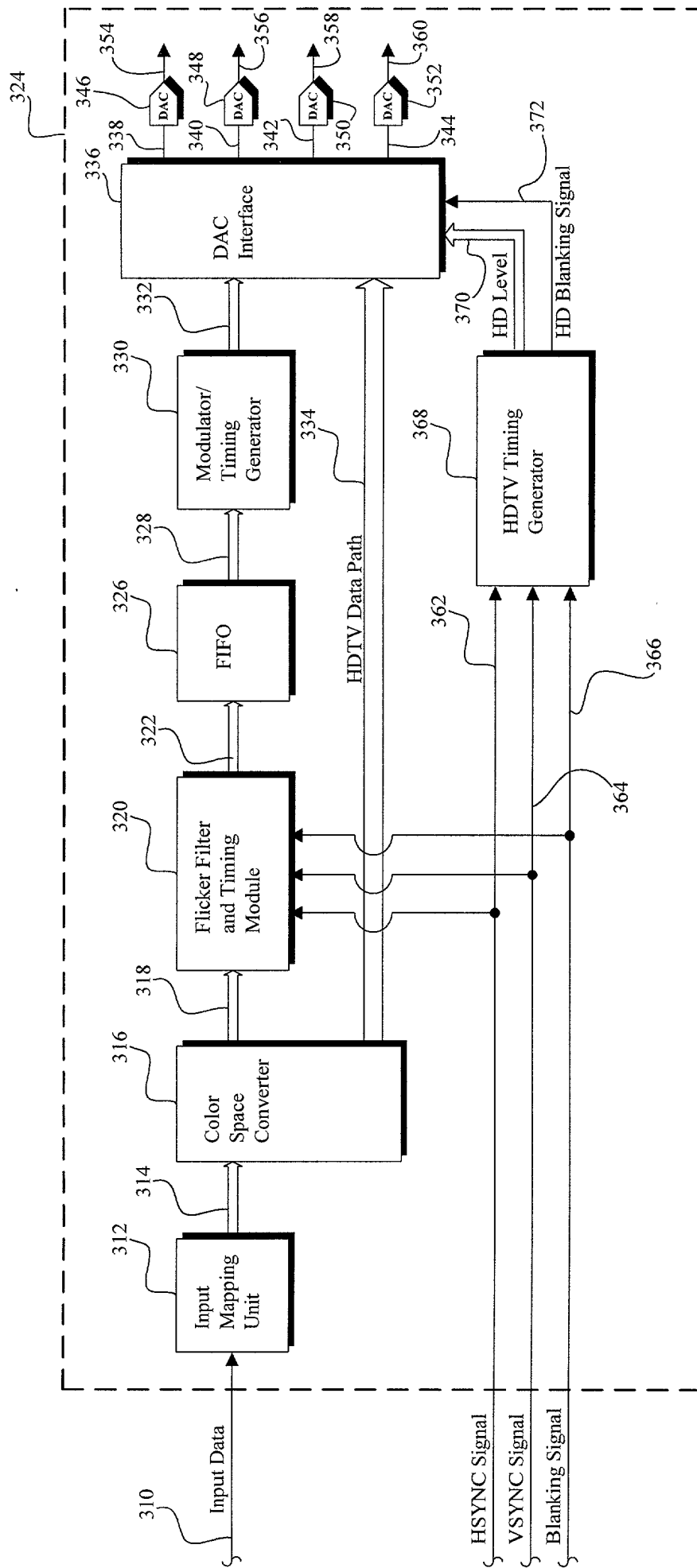


Fig. 3



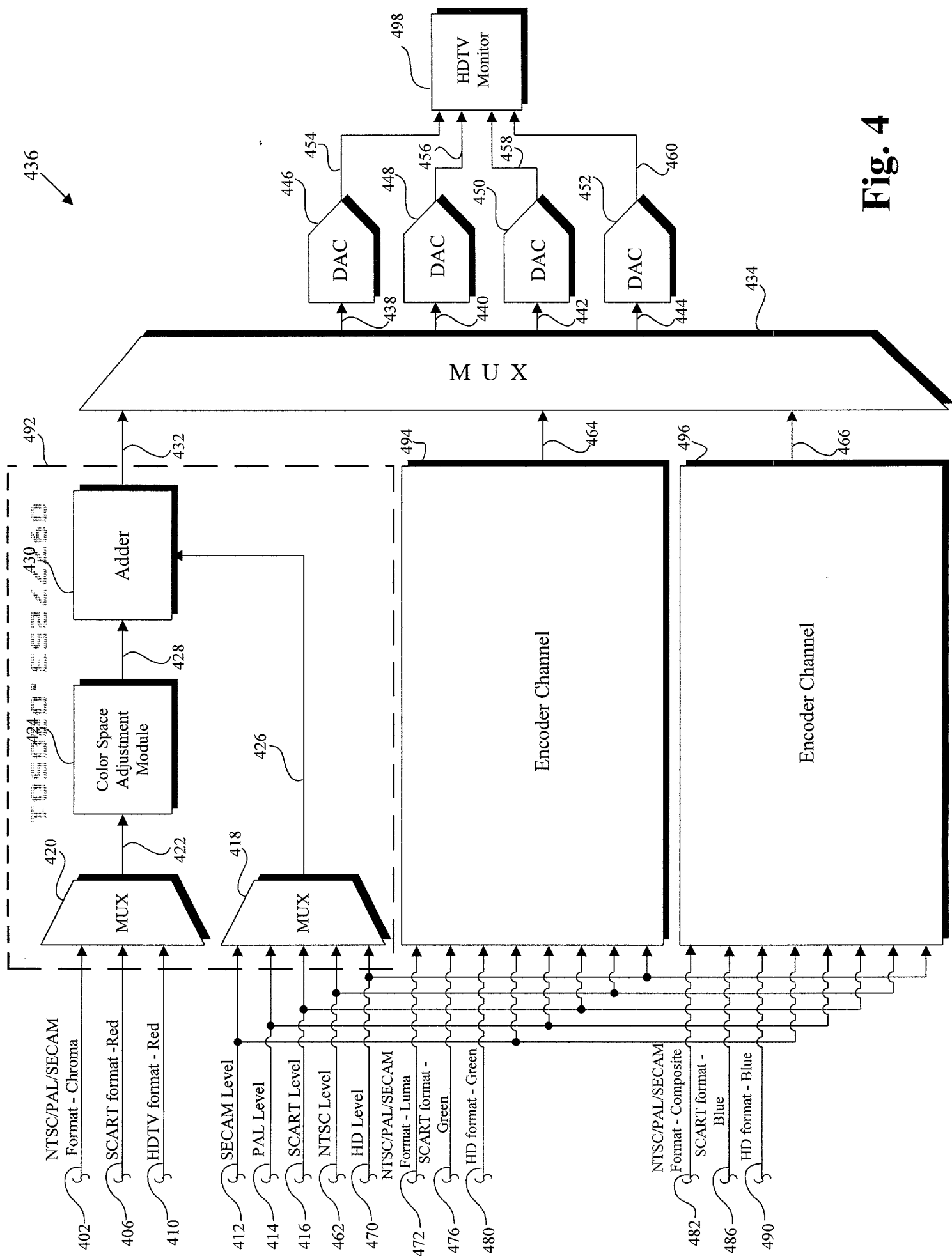


Fig. 4

Fig. 5

